Amendments to the Claims

Claim 1 (Currently amended): A method of forming a transistor device, comprising:

providing a silicon-comprising surface;

exposing the silicon-comprising surface to activated nitrogen to form a peak nitrogen concentration within the silicon-comprising surface of at least 15% (atom percent), the exposing forming a material comprising silicon and nitrogen;

providing a channel region on one side of the material comprising silicon and nitrogen;

providing a transistor gate structure on a side of the material comprising silicon and nitrogen that is opposed to said one side; and

forming a pair of source/drain regions separated from one another by the channel region.

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Claim 2 (Original): The method of claim 1 further comprising forming a layer of silicon dioxide over the channel region, and wherein the silicon-comprising surface is a surface of the silicon dioxide.

Claim 3 (Original): The method of claim 1 wherein the transistor device is a PMOS device.

Claim 4 (Original): The method of claim 1 wherein the transistor device is an NMOS device.

Claim 5 (Original): The method of claim 1 further comprising subjecting the material comprising silicon and nitrogen to an anneal at a temperature of about 900°C for a time of from about 10 seconds to about 60 seconds; and wherein the material comprising silicon and nitrogen is heated to the anneal temperature by rapid thermal processing at a temperature ramp rate of at least about 10°C/second.

Claim 6 (Original): A method of forming a transistor device, comprising:

providing a silicon-comprising surface;

exposing the silicon-comprising surface to activated nitrogen for at least about 20 seconds to convert the silicon-comprising surface to a material comprising silicon and nitrogen; the activated nitrogen being formed by exposing a nitrogen-containing precursor to a plasma maintained at a power of at least about 750 watts;

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providing a channel region on one side of the material comprising silicon and nitrogen;

providing a transistor gate structure on a side of the material comprising silicon and nitrogen that is opposed to said one side; and

forming a pair of source/drain regions separated from one another by the channel region.

Claim 7 (Original): The method of claim 6 further comprising forming a layer of silicon dioxide over the channel region, and wherein the silicon-comprising surface is a surface of the silicon dioxide.

Claim 8 (Original): The method of claim 6 wherein the transistor device is a PMOS device.

Claim 9 (Original): The method of claim 6 wherein the transistor device is an NMOS device.

Claim 10 (Original): The method of claim 6 wherein the plasma is maintained at a power of from about 1,500 watts to about 5,000 watts.

Claim 11 (Original): The method of claim 6 wherein the plasma is remote relative to the silicon-comprising surface.

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Claim 12 (Original): The method of claim 6 wherein the plasma contacts the silicon-comprising surface.

Claim 13 (Original): The method of claim 6 further comprising maintaining the silicon-comprising surface at a temperature of from about 25°C to about 400°C during the exposing of the surface to the activated nitrogen.

Claim 14 (Original): The method of claim 6 further comprising subjecting the material comprising silicon and nitrogen to an anneal at a temperature of about 900°C for a time of from about 10 seconds to about 60 seconds.

Claim 15 (Original): The method of claim 6 further comprising subjecting the material comprising silicon and nitrogen to an anneal at a temperature of about 900°C for a time of from about 10 seconds to about 60 seconds; and wherein the material comprising silicon and nitrogen is heated to the anneal temperature by rapid thermal processing at a temperature ramp rate of at least about 10°C/second.

Claims 16 (Original): A method of forming a transistor device, comprising:

providing a semiconductor substrate having a silicon-comprising surface;

exposing the silicon-comprising surface to activated nitrogen for at least about 20 seconds to convert the silicon-comprising surface to a material comprising silicon and nitrogen; the activated nitrogen being formed by exposing a nitrogen-containing precursor to a plasma maintained at a power of at least about 750 watts;

forming a transistor gate structure over the material comprising silicon and nitrogen; the transistor gate structure being formed proximate a channel region; the material comprising silicon and nitrogen being between the transistor gate structure and the channel region; and

forming a pair of source/drain regions separated from one another by the channel region.

Claim 17 (Original): The method of claim 16 further comprising forming a layer of silicon dioxide over the channel region, and wherein the silicon-comprising surface is a surface of the silicon dioxide.

Claim 18 (Original): The method of claim 16 wherein the transistor device is a PMOS device.

Claim 19 (Original): The method of claim 16 wherein the transistor device is an NMOS device.

Claim 20 (Original): The method of claim 16 wherein the plasma is maintained at a power of from about 1,500 watts to about 5,000 watts.

Claim 21 (Original): The method of claim 16 wherein the plasma is remote relative to the silicon-comprising surface.

Claim 22 (Original): The method of claim 16 wherein the plasma contacts the silicon-comprising surface.

Claim 23 (Original): The method of claim 16 further comprising maintaining the silicon-comprising surface at a temperature of from about 25°C to about 400°C during the exposing of the surface to the activated nitrogen.

Claim 24 (Original): The method of claim 16 further comprising subjecting the material comprising silicon and nitrogen to an anneal at a temperature of about 900°C for a time of from about 10 seconds to about 60 seconds.

Claim 25 (Original): The method of claim 16 further comprising subjecting the material comprising silicon and nitrogen to an anneal at a temperature of about 900°C for a time of from about 10 seconds to about 60 seconds; and wherein the material comprising silicon and nitrogen is heated to the anneal temperature by rapid thermal processing at a temperature ramp rate of at least about 10°C/second..

Claim 26 (Currently amended): A method of forming a transistor device, comprising:

providing a silicon-comprising material;

defining a channel region of the transistor device beneath the silicon-comprising material;

implanting a dopant into the channel region to a concentration of less than about 7×10^{17} atoms/cm^3 as a V_t implant;

forming a dielectric material over the channel region; the forming of the dielectric material comprising exposing the silicon-comprising material to activated nitrogen to form a peak nitrogen concentration within the exposed ~~dielectric~~ silicon-comprising material of at least about 15 atom percent, the dielectric material comprising the exposed silicon-comprising material;

forming a transistor gate structure over the nitrogen-comprising material; and

forming a pair of source/drain regions separated from one another by the channel region.

Claim 27 (Original): The method of claim 26 further comprising forming a layer of silicon dioxide over the channel region, and wherein the silicon-comprising material is the silicon dioxide.

Claim 28 (Original): The method of claim 26 wherein the transistor device is a PMOS device.

Claim 29 (Original): The method of claim 26 wherein the concentration of dopant in the V_t implant is less than 7×10^{17} atoms/cm^3.

Claim 30 (Original): The method of claim 26 wherein the concentration of dopant in the V_t implant is from about 1×10^{17} atoms/cm^3 to 7×10^{17} atoms/cm^3.

Claim 31 (Original): The method of claim 26 wherein the concentration of dopant in the V_t implant is from about 1×10^{17} atoms/cm^3 to 5×10^{17} atoms/cm^3.

Claim 32 (Original): The method of claim 26 wherein the activated nitrogen is formed from a plasma maintained at a power of from about 1,500 watts to about 5,000 watts.

Claim 33 (Original): The method of claim 26 wherein the activated nitrogen is formed from a plasma that is remote relative to the silicon-comprising material.

Claim 34 (Original): The method of claim 26 wherein the activated nitrogen is formed from a plasma that contacts the silicon-comprising material.

Claim 35 (Original): The method of claim 26 further comprising maintaining the silicon-comprising material at a temperature of from about 25°C to about 400°C during the exposing of the material to the activated nitrogen.

Claim 36 (Original): A method of forming a plurality of transistor devices, comprising:

providing a semiconductor substrate having a silicon-comprising surface;

defining a plurality of transistor device channel region locations beneath the silicon-comprising surface; the channel region locations being divided amongst a first group and a second group;

covering the silicon-comprising surface over the second group of transistor device channel region locations with a masking material;

while the masking material is over the second group of transistor device channel region locations, exposing the silicon-comprising surface over the first group of transistor device channel region locations to activated nitrogen for at least about 20 seconds to convert the silicon-comprising surface to a material comprising silicon and nitrogen; the activated nitrogen being formed by exposing a nitrogen-containing precursor to a plasma maintained at a power of at least about 750 watts;

removing the masking material;

after removing the masking material, forming transistor gate structures over the first and second groups of transistor device channel region locations; and

forming a plurality of source/drain regions; individual pairs of the source/drain regions being separated from one another by individual channel region locations.

Claim 37 (Original): The method of claim 36 further comprising forming a layer of silicon dioxide over the channel region locations, and wherein the silicon-comprising surface is a surface of the silicon dioxide.

Claim 38 (Original): The method of claim 36 wherein the transistor devices are all PMOS devices.

Claim 39 (Original): The method of claim 36 wherein at least some of the transistor devices are NMOS devices.

Claim 40 (Original): The method of claim 36 wherein the plasma is maintained at a power of from about 1,500 watts to about 5,000 watts.

Claim 41 (Original): The method of claim 36 wherein the plasma is remote relative to the silicon-comprising surface.

Claim 42 (Original): The method of claim 36 wherein the plasma contacts the silicon-comprising surface.

Claim 43 (Original): The method of claim 36 further comprising maintaining the silicon-comprising surface at a temperature of from about 25°C to about 400°C during the exposing of the surface to the activated nitrogen.

Claims 44-60 (Cancelled).

Claim 61 (New): A method of forming a plurality of transistor devices comprising:

providing a substrate having a surface, the surface comprising silicon;

incorporating at least 15% (atom percent) nitrogen into the surface by exposing the surface to activated nitrogen;

forming a pair of source/drain regions within the substrate, the pair of source/drain regions being separated from one another by a channel region, wherein each of the source/drain regions comprises a heavily doped portion proximate the channel region and a lightly doped portion separated from the channel region by the heavily doped portion; and

providing a transistor gate structure over both the surface and the channel region.

Claim 62 (New): The method of claim 61 wherein the surface consists essentially silicon.

Claim 63 (New): The method of claim 61 wherein the surface consists of silicon.

Claim 64 (New): The method of claim 61 wherein the incorporating comprises forming the activated nitrogen by exposing a nitrogen precursor to a plasma.

Claim 65 (New): The method of claim 61 wherein the surface has a thickness of less than 10 Å.

Claim 66 (New): The method of claim 61 wherein the transistor device is a PMOS device.

Claim 67 (New): The method of claim 61 wherein the transistor device is an NMOS device.